DOI: 10.15415/mjis.2014.22010

Simulated Annealing Approach onto VLSI Circuit Partitioning

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Abstract Decompositions of inter-connected components, to achieve modular independence, poses the major problem in VLSI circuit partitioning. This problem is intractable in nature, Solutions of these problem in computational science is possible through appropriate heuristics. Reduction of cost that occurs due to interconnectivity between several VLSI components is referred in this paper. Modification of results derived by classical iterative procedures with probabilistic methods is attempted. Verification has been done on ISCAS-85 benchmark circuits. The proposed design tool shows remarkable improvement result in comparison to the traditional one, when applied to the standard benchmark circuits like ISCAS-85.

Keywords: Circuit Partitioning, Intractability, Metaheuristics, Randomized search, Simulated Annealing.

1. INTRODUCTION

The technology of VLSI consists of fabrication of large number of components within a tiny space. Complex systems like this raise the challenge to get designed in an efficient way. So it is required for the systems to partition into smaller sub-systems to be configured properly. Decompositions of inter-connected components, to achieve modular independence, create the major problem of circuit partitioning. In VLSI design, this problem is intractable in nature. The major objective of partitioning a circuit is to achieve concurrency in VLSI system design, preserving the original functionality of the system. In VLSI circuit partitioning, large circuits are partitioned into smaller components to attain minimal connectivity amongst them. Cost of intermodule connectivity and the relevant circuital delay are the key parameters in designing complex VLSI system. The interconnections between different modules are referred as cutsizes. The goal of partitioning is to minimize the cutsize.

Mathematical Journal of Interdisciplinary Sciences
Vol. 2, No. 2,
March 2014
pp. 133–139

To solve this kind of problem is inapplicable in nature. As the number of permutation would reveal an exponential function, the problem is computationally hard and hence required some heuristics to come across a near optimal solution.

Earlier on **Kernighan and Lin (1970)** proposed an iterative solution to solve bipartitioning. The approach includes swapping of most suitable pair of components per iteration, until no improvements shown. This ensures local optimum solutions for the standard benchmark circuits.

After a few years, **Fiduccia and Mattheyses** (1982) modified the earlier approach by adjusting the algorithmic complexity. It was also an iterative method that selects a single vertex to swap at one instance. In this method the most suitable vertex of a partition is chosen, the most suitable one from the other partition is chosen next. The method continues until no more vertex is left.

Apart from these two well known heuristics, a number of heuristics have been applied to solve the partitioning problem. Genetic Algorithm, Ant Colony Optimization, Simulated Annealing are some of them.

In this work, a probabilistic version of simulated annealing is used. The FM method is used to obtain feasible solutions needed in this approach. When applied to the standard **benchmark circuits** (like **ISCAS-85**) the heuristic is found to give better results compare to other heuristics.

2. PROBLEM FORMULATION

The problem is related to reorientation of components in a circuit. It is a tedious task to do the same physically. Mapping the problem into the domain of graph theory makes it easier to deal with. To represent a circuit in a graph, the components and the inter-connections between them are considered as *Vertices* and the *Edges*. A graph G = (V, E), consists of V as the set of vertices and E as the set of edges. Here in this problem the components $\{v_1, V_2, ..., v_n\} \in V$ and their interconnections as set of edges $\{e_1, e_2, ..., e_n\} \in E$. Thus dividing the elements of V to create disjoint subsets, i.e. $V_i \cap V_j = \varnothing$, where $i \neq j; \cup_{i=1}^{k} V_i = V$, to obtain reduced cutsize, essentially becomes the issue. The total cutcost is sum of C_{ij} where i≠j and C_{ij} stands for the cutcost between partition V_i and V_j.

This approach obtains a biequipartition through FM algorithm, starting with a random partition. Then it starts modifying that solution by Simulated Annealing with various initial temperatures, cooling rates, and equilibrium conditions. The final outcome is the best among them.

3. METHODOLOGY

Simulated Annealing is a probabilistic search technique that maps the chemical annealing process to algorithmic domain. The annealing process

initiates with a high temperature and drastically cooled down to form crystals. Identically, an entity from the solution space of the partitioning problem is taken as an initial state and some amount of iterations are carried through. At every temperature, the process continues to reach the equilibrium at that very temperature. In course of the process, new solutions are generated and checked if a better solution has arrived or not, if the better solution is found, it is kept otherwise a selection procedure takes place. The solution procedure depends on probabilistic criteria. The solutions which fails to match the criteria, are rejected otherwise, they are given a scope to reorient themselves. Thus as the swapping events are carried on at each step there is a high possibility to jump over the local optima and step into another. The entire procedure is highly dependent on the parameters such as initial temperature, initial permutation, cooling rate, equilibrium condition.

Initial temperature: It relates to the value to which the object would be heated in annealing process. Basically, it is the number of iterations of the outer loop in the heuristic. This parameter has crucial effects in case of acceptance of solutions. So it should be maintained carefully. The value of initial temperature must be large enough to enable the algorithm to move off local minima. In this work multiple values have been taken to start off, considering the nature of benchmark, under observation.

```
Algorithm Simulated Annealing
begin
t = t0
current_part = initial_part;
current_score = SCORE(current_part);
repeat
        repeat
        comp1 = SELECT(part1);
        comp2 = SELECT(part2);
        trial_part =
XCHANGE(comp1,comp2,current_part);
        trial_score = SCORE(trial_part);
        ds =( trial_score – current_score);
        if (ds < 0) then
                current_score = trial_score;
                current_part = MOVE(comp1,comp2);
        else
                r = RANDOM(0,1);
                if (r < e-ds/t) then
                        current_score = trial_score;
                        current_part =
MOVE(comp1,comp2);
        until(equilibrium at t is reached)
        t = at (* 0 < a < 1 *);
until (freezing point is reached)
```

Initial permutation: It defines an instance from the solution space, with which the procedure commences. Modifications made on that instance leads to the arrival of a technically good solution. In our work, initial permutation is the solution derived from FM algorithm.

Cooling rate: Decrement of temperature per iteration is controlled by the cooling rate. This is also very significant to perform a successful search. It is implemented by the following rule; $t_{i+1} = s * t_i$, where $s < 1$. In our work, the choice of s has been made in three levels: low, medium and high and ultimately fixed after a series of observations.

Equilibrium condition: At a particular temperature the process attains an equilibrium state. In SA, it is the iteration number of inner loop at every specific temperature. It can be constant or it can be varied with the size of the search space.

The idea of the approach is represented in *Figure-1*. The important feature of S A is to move from local optimum based on the acceptance rule by probable tions. If the current solution minimizes the cutsize,then it is accepted otherwise, a probabilistic calculation as:

$$r < e^{-(trial\ score - current\ score)/t}$$

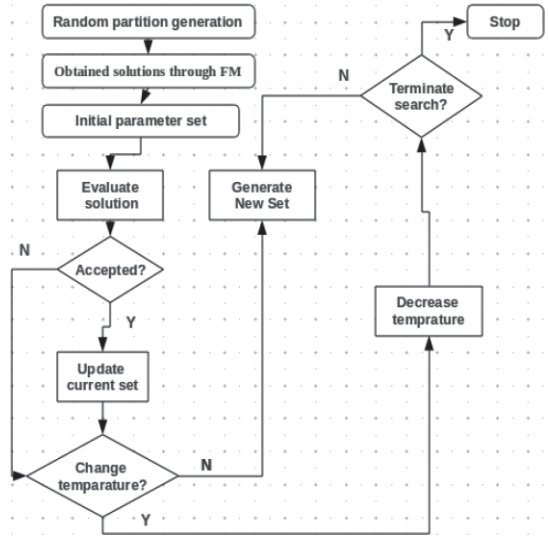


Figure 1: Refiner Flowchart

where r is a random number in [0, 1] andt is the temperature; is made to check the potential of the newly arrived solution

4. RESULTS AND DISCUSSION

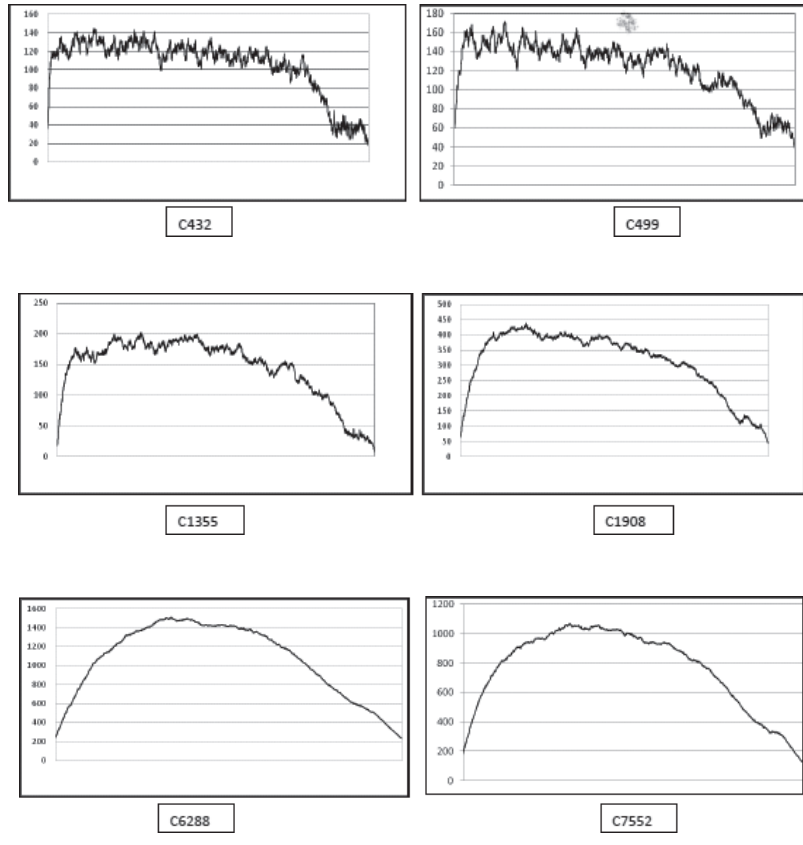
Combinational circuits with reasonable size from **ISCAS-85** benchmark family has been put under observation. Files with even number of components have been tested in as we are searching bipartitions of equal size. Final temperature i.e. the stopping criterion of SA procedure has been changed as per the cardinality of the circuits to control the number of outer loop iterations. Other parameters remained constant in this experiment for now. As the process progresses we have noticed that the initial permutation, the outcome of FM, has been modified to produce better cutsizes. The result table in Figure-2 stands

Initial Temp: 200; Cooling Rate:0.90 Initial Equilibrium: 20; Increment: 2 Benchmark:: Component Numbers	Final Temperature	Initial Cutsize (FM)	Final Cutsize (SA)	Savings (%)	Time (Sec.) Processor speed (3.06GHz)
C432 :: 160	3×10^{4}	37	18	51.35	31
		41	20	51.21	35
	3×10^{6}	42	18	57.14	45
C499::202	3×10^{4}	60	38	36.67	32
		61	39	36.06	38
	3×10^{J}	58	40	31.03	30
	3×10^{4}	13	6	53.84	65
C1355::546		12	8	33.33	68
		17	6	64.71	73
C1908::880	3×10^{4}	64	44	31.25	67
	$3\times10'$	48	38	20.83	62
	3×10^{4}	52	49	5.77	64
C6288::2416	3×10^{6}	150	133	11.33	981
		153	134	12.41	741
		172	122	29.07	1121
C7552 ::3512	3×10^{6}	239	231	3.35	1251
	3×10^{7}	233	198	15.02	1668
		221	190	14.02	2116
	Average Savings = 31.027				

Figure 2

for the efficiency of our concept. Initial cutsize and the final one have been compared after each round of study. The parameters and an approximated time of convergence have been tracked in as well. In each case we can see there is a successful refinement of FM output.

The slope depicted in the graphs conveys the working principle of S A at a glance. Cutsizes are increased at first phases and then they are reduced. Horizontal axis signifies time and vertical is representing cutsize.



Converging time of this SA approach is relatively a bit higher than its counterparts. Other parameters like equilibrium condition, cooling rate could be also changed for carrying on the process. In fact, being an empirical study, these approaches demand several values of different aspects to be tried on. However, with a motivation to check more and more entities from solution space we have achieved some satisfactory results which were intended in this venture.

5. CONCLUSION

In this work, circuit partitioning in VLSI has been mentioned. The results show that on average 31.027 percent savings are made, which is delightful to quite an extent. Further improvements can be made by changing the parameters. We would like to extend this project to suggest a good set of parameters for approaches of these kinds of metaheuristics. A comparison and add-on of existing heuristics for the addressed problem can also be a good one to examine.

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